Morteza Gholipour

Associate Professor

E-mail: gholipour.m@gmail.com
Phone: +981135501441
Address: Dept. of ECE, Babol Noshirvani University of Technology, Babol, Iran

EDUCATION

Ph.D., Electrical and Computer Engineering 2009 – 2014
University of Tehran, Tehran, Iran
M. S., Electrical and Computer Engineering 2000 – 2003
University of Tehran, Tehran, Iran
B. S., Electrical Engineering 1996 – 2000
Ferdowsi University of Mashhad, Mashhad, Iran

VISITING RESEARCH

Visiting Scholar December 2012 – August 2013
Coordinated Science Laboratory, **University of Illinois at Urbana-Champaign**, Champaign, IL, USA

- Physics-based modeling of the newly proposed graphene-based transistors; compact SPICE modeling.
- Released the open-source graphene transistor model on nanohub.org. (1180+ downloads since 2014.)
- Performance evaluation compared to conventional CMOS transistors.

SKILLS AND LANGUAGES

- Python, C/C++, HSPICE, Modelsim, Leonardo Spectrum, Tanner L-EDIT, MATLAB, Orcad, Protel, Quartus, Virtual NanoLab, Silvaco TCAD, FPGA tools, Assembly Language Programming, VHDL and Verilog Languages, Visual Basic, Visual C++, Office software tools.
- Persian (native), English (professional working proficiency)

RESEARCH EXPERIENCE

Nanoelectronics and digital system design 2020 – present

- Memory cell design
- Nano device modeling and simulation
- Memristor modeling

Modeling and simulation of 2-D material-based devices 2017 – 2020

- Compact modeling of TMDFET devices
- SPICE compact model of Schottky- and MOS-type GNRFET devices

Modeling and simulation of crossbar-based nano structures 2012 – 2017

- Proposed graphene-based nano-crossbar architecture for electronics circuit design.
- Modeling and performance exploration of the nano-crossbar architecture.

Modeling of carbon nanotube as chips interconnects 2011 – 2012

- Proposed a compact RC model for multi-walled carbon nanotube interconnects; exploration of buffer insertion and crosstalk effects on the CNT interconnects.

Designing asynchronous logic control 2002 – 2003

- Proposed a low latency asynchronous design scheme; investigation and simulation of different asynchronous logic designs; performance exploration.

WORK EXPERIENCE

Hardware designer and software developer, 2001 – 2005

Research institute for ICT (formerly Iran Telecommunication Research Center), Tehran, Iran

- Implemented management protocol for Synchronous Digital Hierarchy (SDH). **(C++)**
- Implemented SDH Equipment Management Function (SEMF) interface. **(C++)**
- Designed and implemented High-Level Data Link Control (HDLC) hardware and firmware for SDH system. **(Verilog)**

ACADEMIC EXPERIENCE

Faculty Member, Babol Noshirvani University of Technology, Babol, Iran 2014 – present

Deputy, Office of Scientific Collaborations and International Affairs (2023-present)

Visiting Scholar (Advisor: Prof. Deming Chen of University of Illinois at Urbana-Champaign) 2012 – 2013

Advanced VLSI Design, Nanoelectronics, Quantum Electronics, Advanced Digital Electronics, Computer Architecture.

Faculty Member, Azad University of Behshahr, Behshahr, Iran 2005 – 2009

- Lecturer of: C++ programming, Pascal programming, Electronics, Computer Networks, Digital Logic Circuits, Digital System Design Laboratory, Microprocessor laboratory.
- FPGA implementation of the lifting based wavelet transform for image processing applications, using Verilog language.

Reviewer, IEEE *Transactions on Computer-Aided Design of Integrated Circuits and Systems*, IEEE *Transactions on Very Large Scale Integration Systems*, *IEEE Transactions on Electron Devices, IEEE Transactions on Nanotechnology, Microelectronics Journal*, *Journal of Low Power Electronics, Journal of Computational Electronics, Microelectronics Reliability Journal, International Journal of Electronics and Communications, International Journal of Circuit Theory and Applications, Journal of Emerging Technologies in Computing Systems*.

COURSES TAUGHT

Undergraduate

- Digital systems I (Logic circuits)
- Digital systems II (computer architecture)
- Electronics II
- Pulse technique
- Microprocessors

Graduate

- Advanced digital electronics
- Advanced VLSI
- Quantum electronics
- Nanoelectronics
- Designing special processors

PUBLICATIONS

Journal papers

- E. Abbasian, E. Mani, **M. Gholipour**, M. Karamimanesh, M. Sahid, A. Zaidi, "A Schmitt-Trigger-Based Low-Voltage 11 T SRAM Cell for Low-Leakage in 7-nm FinFET Technology," *Circuits, Systems and Signal Processing*, 41, pp. 3081-3105, 2022.
- E. Abbasian, **M. Gholipour**, "Robust transmission gate-based 10T subthreshold SRAM for internet-of-things applications," *Semiconductor Science and Technology*, 37 085013, pp. 1108–1115, 2022.
- E. Gholinataj-Jelodar, A. Aghanejad Ahmadchally, A. Gooran-Shoorakchaly, **M. Gholipour**, "Semi-analytical SPICE-compatible ballistic I–V model for 5 nm channel MoS2 FETs," *Journal of Computational Electronics*, 21, pp. 1108–1115, 2022.
- E. Abbasian, **M. Gholipour**, "Design of a Highly Stable and Robust 10T SRAM Cell for Low-Power Portable Applications," *Circuits, Systems, and Signal Processing*, vol. 41, pp. 5914–5932, 2022.
- E. Abbasian, S. Birla, **M. Gholipour**, "A 9T high-stable and Low-Energy Half-Select-Free SRAM Cell Design using TMDFETs," *Analog Integrated Circuits and Signal Processing*, 25, pp. 1-9, 2022.
- E. Abbasian, S. Birla, **M. Gholipour**, "Ultra-low-power and stable 10-nm FinFET 10T sub-threshold SRAM," *Microelectronics Journal*, 123, 105427, 2022.
- E. Abbasian, **M. Gholipour**, S. Birla, "A Single-Bitline 9T SRAM for Low-Power Near-Threshold Operation in FinFET Technology," *Arabian Journal for Science and Engineering*, 25, 2022.
- B. Vakili, **M. Gholipour**, "Enhanced overloaded code division multiple access for network on chip," *IET Computers and Digital Techniques*, 16, pp. 45-53, 2021.
- E. Abbasian, **M. Gholipour**, "Single-ended half-select disturb-free 11T static random access memory cell for reliable and low power applications," *International Journal of Circuit Theory and Applications*, 49, pp. 970-989, 2021.
- E. Abbasian, S. Birla and **M. Gholipour**, "A Comprehensive Analysis of Different SRAM Cell Topologies in 7-nm FinFET Technology," *Silicon*, Oct. 2021 https://doi.org/10.1007/s12633-021-01432-6.
- E. Abbasian, **M. Gholipour**, F. Izadinasab, "Performance evaluation of GNRFET and TMDFET devices in static random access memory cells design," *Int J Circ Theor Appl*. 2021, 49(11), 3630- 3652.
- F. Izadinasab, **M. Gholipour**, "Half-select disturb-free single-ended 9-transistor SRAM cell with bit-interleaving scheme in TMDFET technology," *Microelectronics Journal*, 113: 105100, 2021.
- E. Abbasian, **M. Gholipour**, "Design of a Schmitt-Trigger-Based 7T SRAM cell for variation resilient Low-Energy consumption and reliable internet of things applications," AEU-International Journal of Electronics and Communications, 138:153899-, 2021.
- E. Abbasian, and **M. Gholipour**, "Single-ended half-select disturb-free 11T SRAM cell for reliable and low power applications," to be appeared in *International Journal of Circuit Theory and Application*, 2021.
- A. Gooran-Shoorakchaly, A. Aghanejad Ahmadchally, S. Soleimani-Amiri, and **M. Gholipour**, "Design of a Low-Power Short-Channel Electrostatically-Doped Silicene Nanoribbon FET," to be appeared in *IEEE Transactions on Electron Devices*, 2021.
- A. Aghanejad Ahmadchally, **M. Gholipour**, "Investigation of 6-armchair graphene nanoribbon tunnel FETs," *Journal of Computational Electronics*, 20: 1114 - 1124, 2021.
- E. Mahmoodi, and **M. Gholipour**, "Design space exploration of low-power flip-flops in FinFET technology," *Integration, the VLSI Journal*, vol. 75, pp. 52-62, 2020.
- E. Abbasian, and **M. Gholipour**, "A variation-aware design for storage cells using Schottky-barrier-type GNRFETs," *Journal of Computational Electronics*, vol. 19, no. 3, pp. 987–1001, 2020.
- A. Rezaei, B. Azizollah-Ganji, **M. Gholipour**, "Effects of the Channel Length on the Nanoscale Field Effect Diode Performance," *Optoelectronical Nanostructures*, vol. 3, no.1, 2018.
- **M. Gholipour**, Y-Y. Chen, and D. Chen, "Compact Modeling to Device- and Circuit-Level Evaluation of Flexible TMD Field-Effect Transistors," *IEEE Transactions on Computer Aided Design*, vol. 37, no. 4, April 2018.
- **M. Gholipour**, "A Compact Short-Channel Model for Symmetric Double-Gate TMDFET in Subthreshold Region," *IEEE Transactions on Electron Devices*, vol. 64, no.8, pp. 3466-3469, 2017.
- **M. Gholipour**, Y-Y. Chen, A. Sangai, N. Masoumi, and D. Chen, "Analytical SPICE-Compatible Model of Schottky-Barrier-type GNRFETs with Performance Analysis," *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*,

vol. 24, no. 2, pp. 650-663, Feb. 2016.

- Y-Y. Chen, A. Sangai, A. Rogachev, **M. Gholipour**, G. Iannaccone, G. Fiori, and D. Chen, "A SPICE-Compatible Model of MOS-Type Graphene Nano-Ribbon Field-Effect Transistors Enabling Gateand Circuit-Level Delay and Power Analysis Under Process Variation," *IEEE Transactions on Nanotechnology*, vol. 14, no. 6, Nov. 2015.
- **M. Gholipour**, N. Masoumi, Y-Y. Chen, D. Chen, and M. Pourfath, "Asymmetric Gate Schottky-Barrier Graphene Nanoribbon FETs for Low-Power Design," *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4000-4006, Dec. 2014.
- **M. Gholipour** and N. Masoumi, "Graphene Nanoribbon Crossbar Architecture for Low Power and Dense Circuit Implementations," *Microelectronics Journal*, Volume 45, Issue 11, November 2014, pp. 1533–1541.
- **M. Gholipour**, and N. Masoumi, "Design investigation of nanoelectronic circuits using crossbar-based nanoarchitectures," *Microelectronics Journal*, Volume 44, Issue 3, March 2013, Pages 190–200.
- **M. Gholipour**, and N. Masoumi, "Efficient Inclusive Analytical Model for Delay Estimation of Multi-Walled Carbon Nanotube Interconnects", *IET Circuits Devices Syst.*, July 2012, Volume 6, Issue 4, p.252–259.
- K. Shojaee, **M. Gholipour**, A. Afzali-Kusha and M. Nourani, "Comparative Study of Asynchronous Pipeline Design Methods", *IEICE Electron. Express*, Vol. 3, No. 8, pp.163-171, (2006).

Conference papers

- Y-Y. Chen, **M. Gholipour**, and D. Chen, "Flexible Transition Metal Dichalcogenide Field-Effect Transistors: A Circuit-Level Simulation Study of Delay and Power under Bending, Process Variation, and Scaling," *Asia and South Pacific Design Automation Conference* (*ASP-DAC*), pp.761-768, Jan. 2016.
- H. Sheikhassadi, N. Masoumi, **M. Gholipour**, and M. Rahiminejad, "Time Domain Modeling of Crosstalk Voltage on MWCNT Interconnects," *Iranian Conference on Electrical Engineering* (*ICEE*), pp. 1301-1305, Apr. 2015.
- **M. Gholipour**, Y-Y. Chen, A. Sangai, and D. Chen, "Highly Accurate SPICE-Compatible Modeling for Single- and Double-Gate GNRFETs with Studies on Technology Scaling," *Proceedings of IEEE/ACM Design, Automation & Test in Europe* (*DATE*), Dresden, Germany, March 2014.
- Y-Y. Chen, A. Sangai, **M. Gholipour**, and D. Chen, "Graphene Nano-Ribbon Field-Effect Transistors as Future Low-Power Devices," *Low Power Electronics and Design (ISLPED), 2013 IEEE International Symposium on*, pp. 151-156, 4-6 Sept. 2013.
- Y-Y. Chen, A. Sangai, **M. Gholipour**, and D. Chen, "Schottky-Barrier-Type Graphene Nano-Ribbon Field-Effect Transistors: A Study on Compact Modeling, Process Variation, and Circuit Performance," *2013 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 82-88, Jul. 2013.
- **M. Gholipour**, N. Masoumi, and H. Sheikhassadi, "Analytical Method for Crosstalk Peak Voltage Estimation of MWCNT Interconnects," *21th Iranian Conference on Electric Engineering*, Mashhad, Iran, May 2013.
- **M. Gholipour**, and N. Masoumi, "Efficient Model for Delay Estimation of MWCNT Interconnects," International *Conference on Microelectronics (ICM* 2011), Tunisia, pp. 1-4, Dec. 2011.
- **M. Gholipour**, and N. Masoumi, "A Comparative Study of Nanowire Crossbar and MOSFET Logic Implementations," *EUROCON-IEEE International Conference on Computer as a Tool*, Lisbon, Portugal, pp. 1-4, 2011.
- **M. Gholipour**, H. Ahmadi Noubari, and M. Kamarei, "A DSP Implementation of Lifting Based DWT for Image Processing Applications," *IEEE ICSIP Int. Conf.*, Dec. 2010, Changsha, China.
- **M. Gholipour**, and H. Ahmadi Noubari, "Hardware Implementation of Lifting Based Wavelet Transform," *IEEE ICSPS Int. Conf.*, Jul. 2010, Dalian, China, vol. 1, pp. 215-219.
- **M. Gholipour**, M. Nourani, D. Edwards, and A. Afzali-Kusha, "LLA: A Low Latency Asynchronous Control with applications," *IEEE ISSCS Int. Conf.*, Jul. 2009, Iasi, Romania, pp. 513-516.
- **M. Gholipour**, A. Afzali-Kusha, and M. Nourani, "A Novel Low Latency Asynchronous Pipeline Control Circuit," *Applied Electronics Intl. Conf.*, Sep. 2008, Pilsen, Czech Republic, pp. 53-55.
- **M. Gholipour**, K. Shojaee, A. Afzali-Kusha, A. Khademzadeh and M. Nourani, "An Efficient Model for Performance Analysis of Asynchronous Pipeline Design Methods," *IEEE ISCAS Conf.*, May 2005, Kobe, Japan, pp. 5234-5237.
- **M. Gholipour**, K. Shojaee, A. Khademzadeh, A. Afzali-Kusha and M. Nourani," Performance and Power Analysis of Asynchronous Pipeline Design Methods," *16th IEEE ICM Conf.,* December 2004, Tunis, Tunisia.
  M. Gholipour, A. Afzali-Kusha, M. Nourani and A. Khademzadeh, "An Efficient Asynchronous Pipeline FIFO for Low-Power Applications," *45th IEEE MWSCAS Conf.*, August 2002, Tulsa, Oklahoma, Vol. 2 pp. 481-484.